REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-13 and 15-22 are pending in this application. Claims 1-13 are amended, Claim 14 is cancelled and Claims 15-22 are added by the present response.

The changes to the claims are believed to find support in the disclosure as originally filed and thus are not believed to raise a question of new matter.

In the outstanding Office Action, Claims 1-8 and 12-14 are rejected under 35 U.S.C. §102(e) as anticipated by Admitted Prior Art, herein "APA". Claims 9-11 were objected to as dependent upon a rejected base claim, but were noted as allowable if rewritten in independent form to include all of the limitations of their base claim and any intervening claims.

Initially, Applicants gratefully acknowledge the early indication of the allowable subject matter in Claims 9-11. However, since Applicants consider that Claim 1 as amended patentably defines over the cited art, Claims 9-11 have presently been maintained in dependent form.

Before turning to the outstanding prior art rejections, it is believed that a brief review of the present invention would be helpful.

Claim 1 describes a semiconductor memory comprising "a plurality of memory cell arrays having a plurality of memory cells or memory cell units each of which include a plurality of memory cells, arranged in a matrix, wherein the plurality of memory cell arrays are located independently of each other and have a plurality of cell array groups each of which includes two or more different memory cell arrays, a first Pass/Fail signal indicative of success or failure of an operation is outputted in accordance with each cell array group, and the semiconductor memory device is a memory chip including all of the plurality of memory cell array groups." Newly added Claim 15 recites analogous features.

For example in Figure 9, Array 0 and Array 4 could form one group as they are different arrays.

Thus, in Figure 9, the group including Array 0 and Array 4 outputs one Pass/Fail signal. For example, as described in the specification on page 8, line 12 to page 9, line 16, a 2-Gbit package product of Figure 9 is designed for two 1-Gbit chips and as such can only process four Pass/Fail signals per chip. Thus, in Figure 9 the pass signal of Array 0 and the pass signal of Array 4 are "or"ed to produce a single pass signal.

The APA, as shown in Fig. 2, describes a system in which a chip is selected (i.e. chip 0) and four pass fail signals are produced. One pass fail signal is produced for each Array. Further, APA describes that when a second chip is selected (i.e. chip 1) four more pass fail signals are produced.

However, the APA does not describe or suggest a plurality of cell array groups each of which includes two or more different memory cell arrays, a first Pass/Fail signal indicative of success or failure of an operation is outputted in accordance with each cell array group and the semiconductor memory device is a memory chip including all of the plurality of memory cell array groups.

In other words, in Fig. 2 the APA describes two chips each of which has four arrays each array producing a pass/fail signal. The outstanding Office Action states on page 3, line 3 that "in the instant case, the upper Array 0 and the lower Array0 would be one cell array ground and the upper Array1 and the lower array 1 would be another cell array group." However, lower Array 0 and upper Array 0 are on different chips, while Claim 1 describes that "the semiconductor memory device is a memory chip including all of the plurality of memory cell array groups." Or in other words, all of the cell array groups are on a single chip.

This is important because the claimed invention, in a non-limiting example, is used to put a single 2GB chip on a package product designed for two single 1GB chips. Accordingly, when the package product does a pass/fail check on the 2GB chip, the 2GB chip must only output 4 pass/fail signals as that is what the package product is expecting (Chip 0 of Fig. 2 only produces four pass/fail signals). However, the 2GB chip has 8 arrays and therefore produces 8 pass/fail signals. Thus, the claimed invention creates groups of arrays and "or's" the pass/fail result from the groups and thus only produces 4 pass/fail signals.

Accordingly, as APA does not describe or suggest that the semiconductor memory device is a memory chip including all of the plurality of memory cell array groups, Applicants respectfully submit that Claims 1 and 15, and claims depending therefrom, patentably distinguishes over the APA.

Therefore, it is respectfully submitted that independent Claims 1 and 15 and Claims 2-13 and 16-22 depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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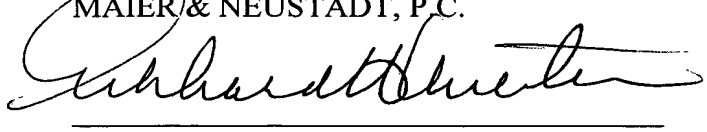

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